**Experiment 2: Half adder and Full adder Implementation in VHDL.**

**Digital Systems Design Lab**

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* **VHDL Source Code for Half Adder and Full Adder:**

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Library ieee;

use ieee.std\_logic\_1164.all;

entity half\_adder is

port(a1,b1:in bit;

sum1,carry1:out bit);

end half\_adder;

entity full\_adder is

port(a2,b2,c2:in bit;

sum2,carry2:out bit);

end full\_adder;

architecture data of full\_adder is

begin

sum2<= a2 xor b2 xor c2;

carry2 <= ((a2 and b2) or (b2 and c2) or (a2 and c2));

end data;

architecture data of half\_adder is

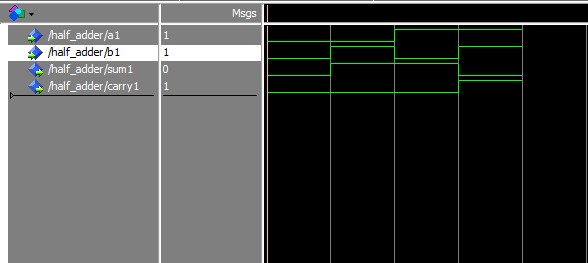
begin

sum1<= a1 xor b1;

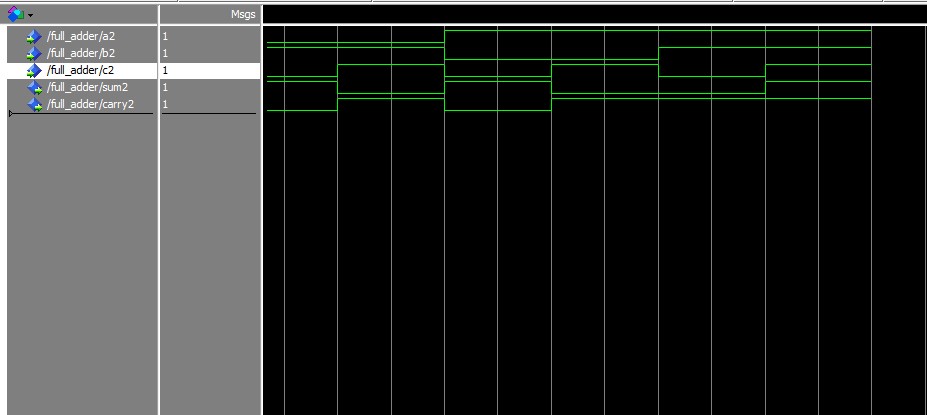
carry1 <= a1 and b1;

end data;

* **Output Waveform of Half Adder:**

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* **Output Waveform of Full Adder:**

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* **Result:**

With the help of this experiment, we are able to understand the behaviour of half adder and full adder digitally.